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FIG.1A

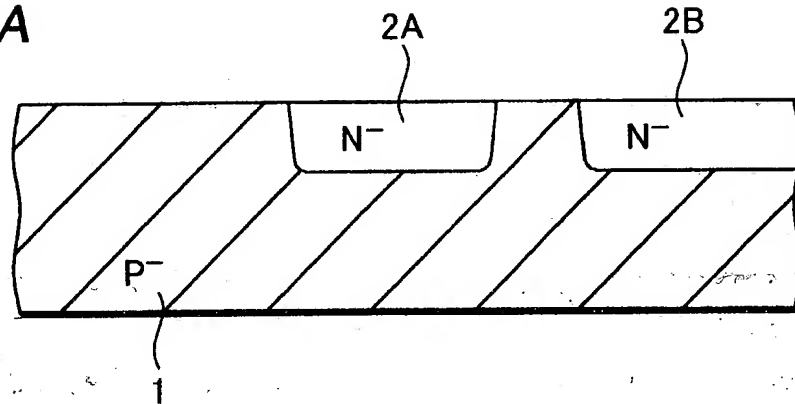


FIG.1B

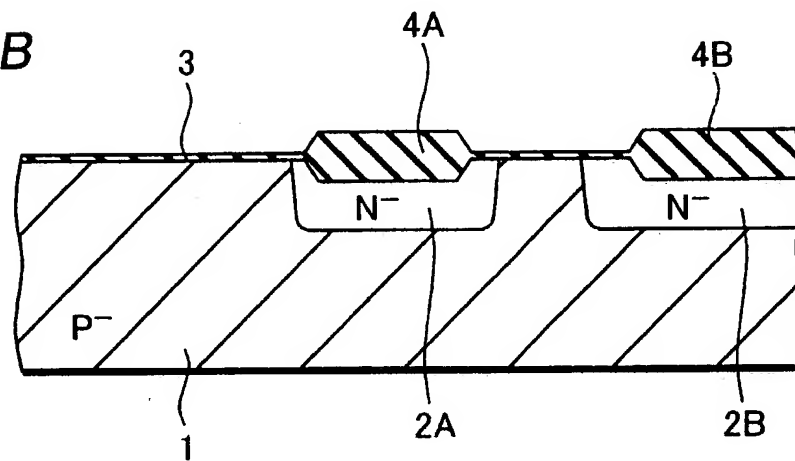
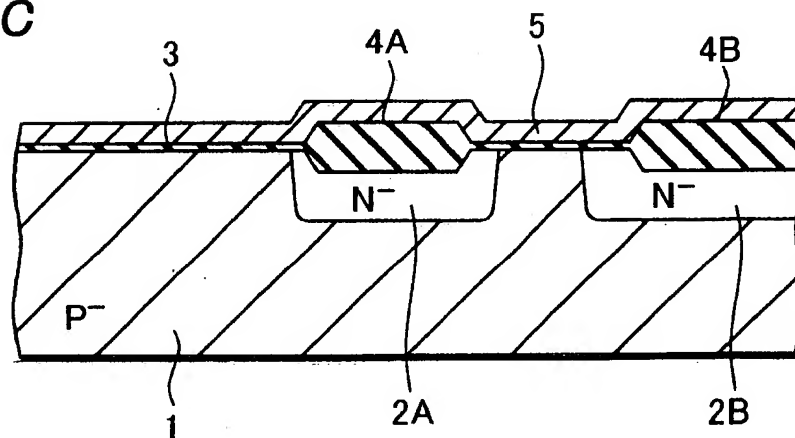


FIG.1C



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FIG.2A

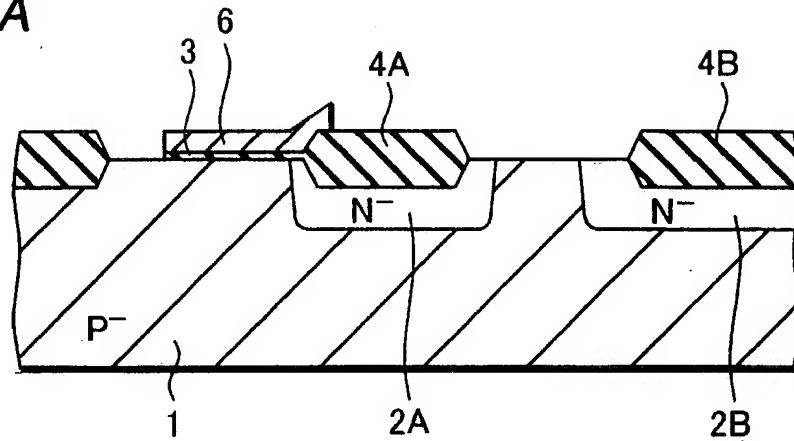


FIG.2B

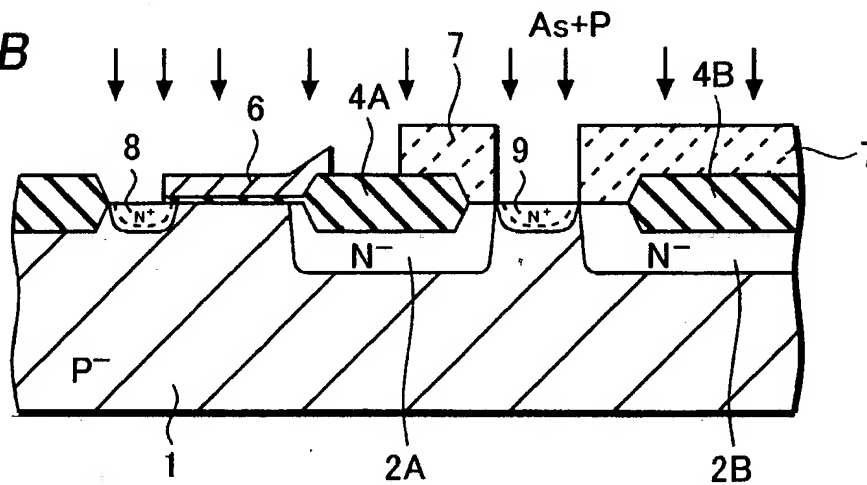


FIG.2C

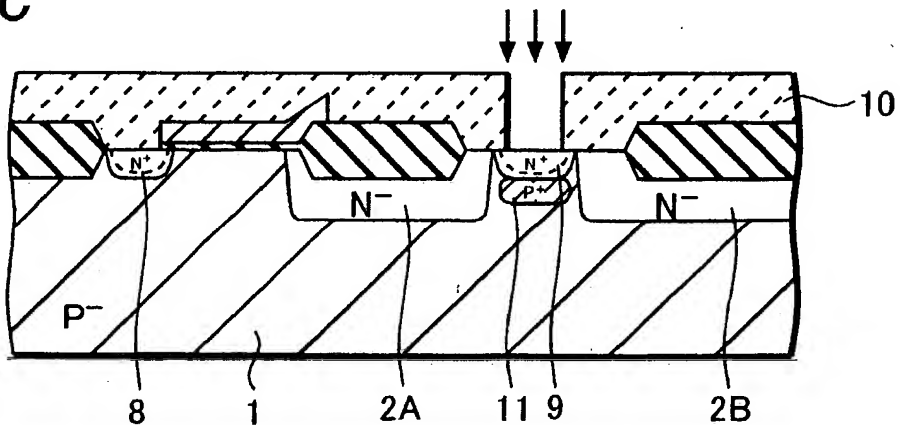


Fig. 1B is a cross-sectional diagram of a semiconductor device. It shows a substrate with a P- region. On top of the substrate, there are several N- regions (labeled 2A and 2B) and one P+ region (labeled 11). A top layer (labeled 12) contains N+ regions (labeled 8 and 9) and a P+ region (labeled 14). The N+ regions are separated by N- regions. The P+ region is located between two N- regions. The diagram is labeled with various numbers: 13, 6, 4, 12, 14, 9, 8, 3, 2A, 11, and 2B.

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FIG.4

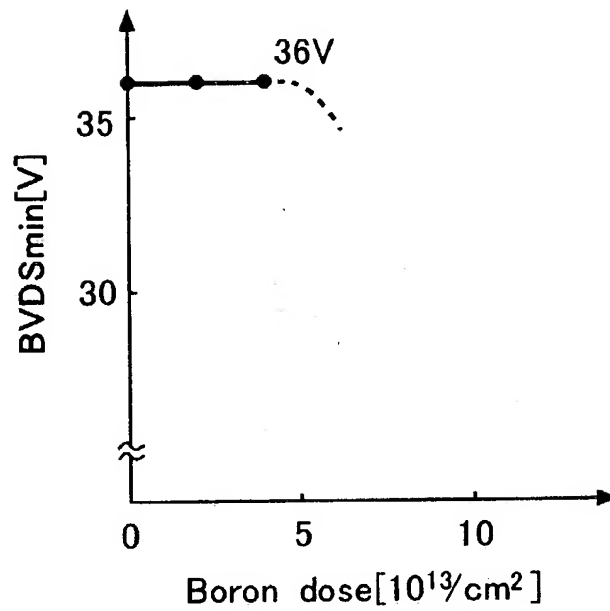
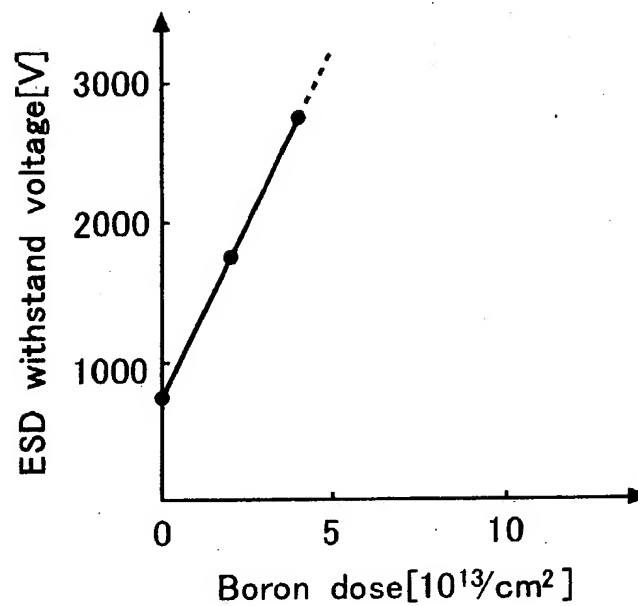


FIG.5



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FIG.6A

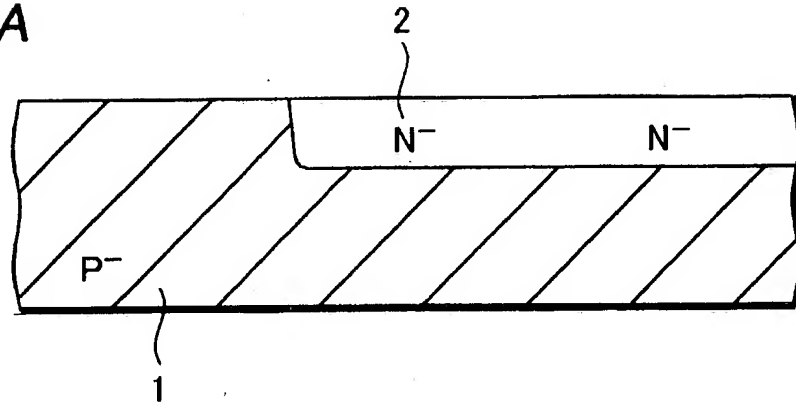


FIG.6B

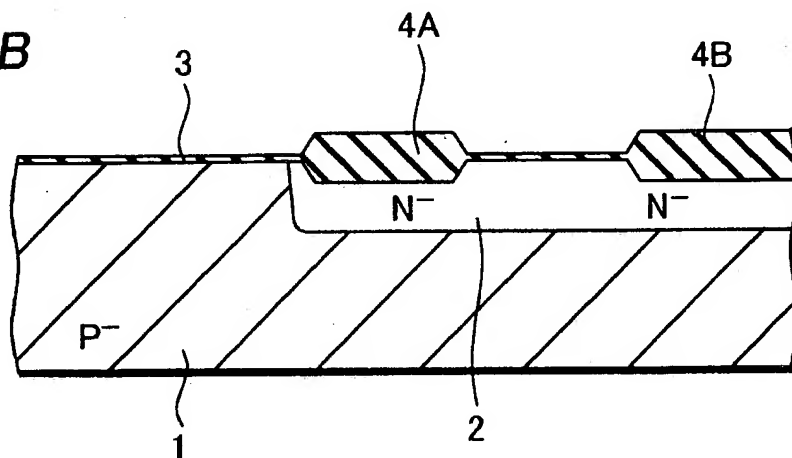
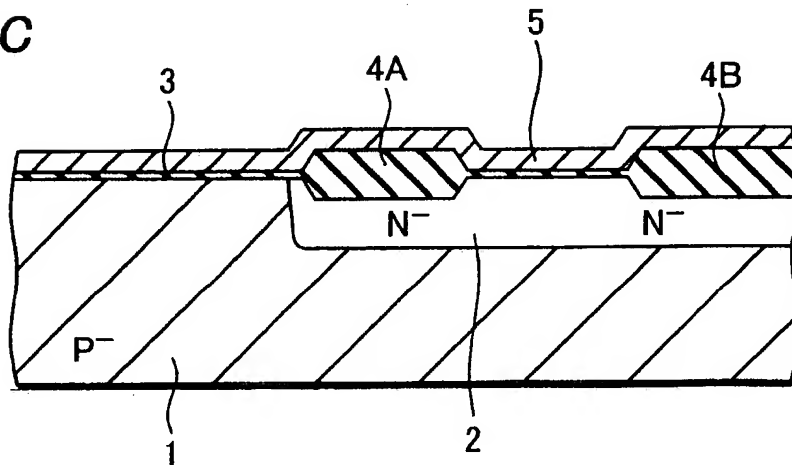


FIG.6C



A cross-sectional view of a semiconductor device. The substrate 1 is a P- type material. A thin layer 2 is formed on the surface. A gate structure 6 is formed on the surface, with a channel region 21 and a source/drain region 2. Arrows A and As indicate incident light or particles.

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FIG.9A

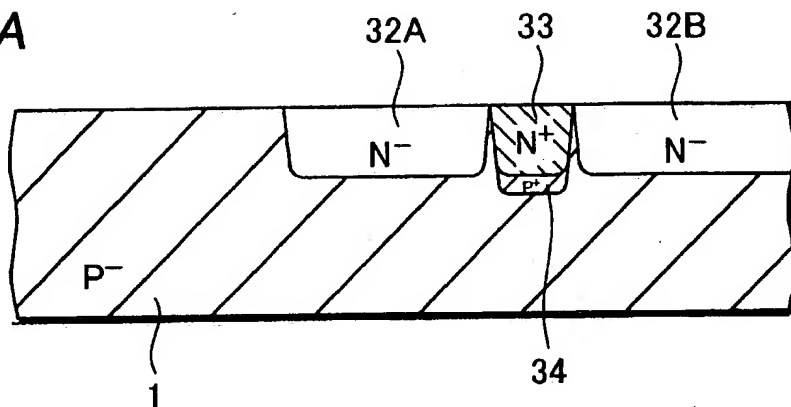


FIG.9B

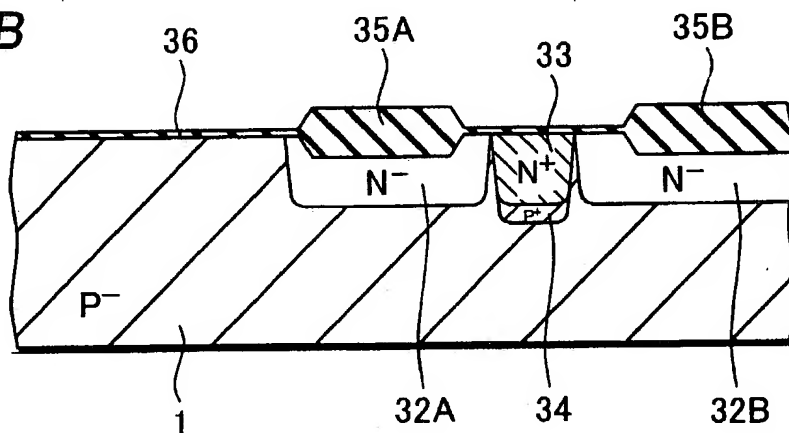
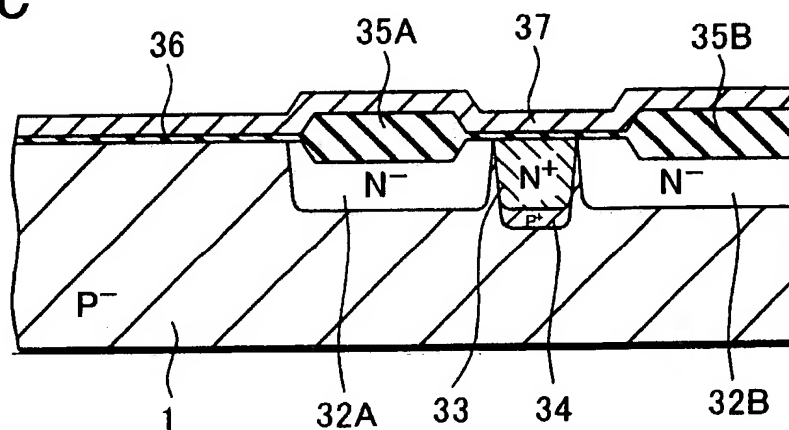


FIG.9C



[illegible][illegible]

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FIG.11

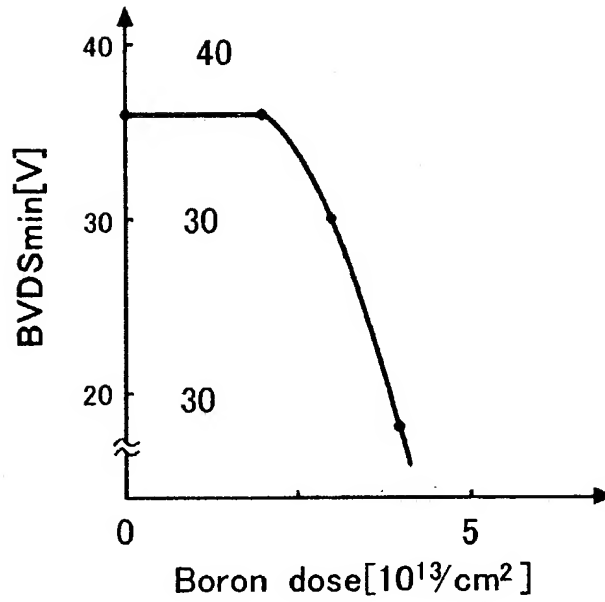


FIG.12

